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Cover Story

Bringing the Intel® Pentium® 4 Processor to Mainstream PCs

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Overview

The Intel® Pentium® 4 processor is Intel's most advanced and powerful desktop processor, and it delivers world-class performance for consumers, business professionals, and entry-level workstation users. While the Pentium 4 processor enhances user experiences with video, speech, 3D, CAD, and other leading-edge applications, it also offers real value for mainstream business users, including improved multitasking productivity and headroom for new applications and operating systems.

The challenge for OEMs is how to deliver the performance of the Pentium 4 processor into the highly cost-sensitive volume mainstream PC market segment. Intel is helping to meet this requirement with the introduction of a new platform based on the Intel® 845 chipset. It allows OEMs and system integrators to combine the benefits of the Pentium 4 processor, including the system-level performance enhancements of the 400-MHz front-side bus (FSB), with the cost-effectiveness of PC133 SDRAM.

In addition to its internal architectural enhancements, the Pentium 4 processor incorporates a series of board-level features for easier, cost-saving designs. For example, Intel's mPGA478 Mechanical Reference Solution provides the on-ramp to Intel's Socket 478 processor roadmap. For details, see the article entitled Moving to Socket mPGA478 Desktop Boards in the September issue of *Intel Developer Update*. Board designs that feature the mPGA478 package provide frequency headroom for the future.

Internal Enhancements

As shown in Figure 1, the Intel 845 chipset is optimized for the Pentium 4 processors at up to 2 GHz and supports the enhanced performance of the processor's 400-MHz FSB. It is important to note that performance PC systems that demand the Pentium 4 processor's maximum data bus bandwidth of 3.2 Gbytes/sec. require the Intel® 850 chipset and RDRAM* memory.

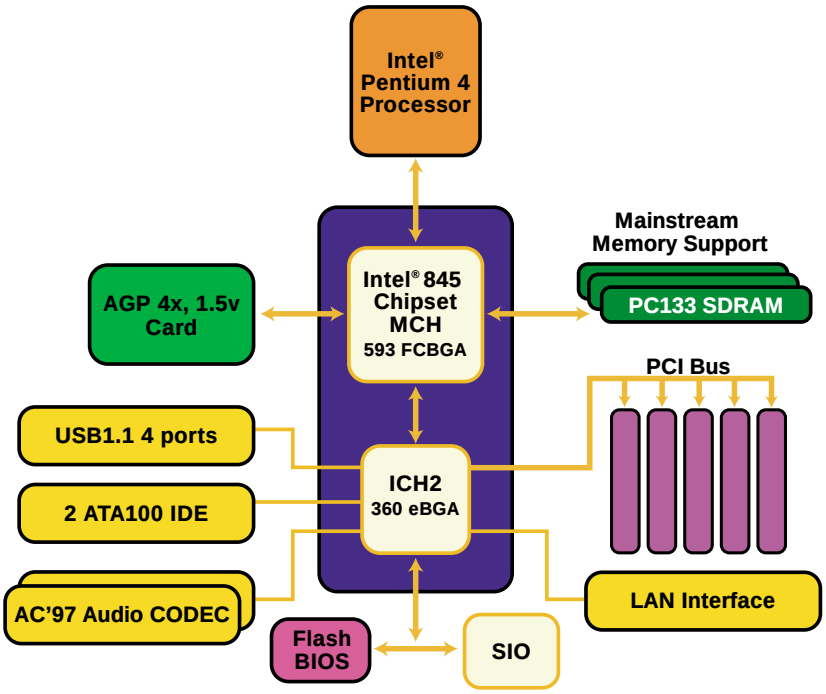

Figure 1. With support for cost-effective PC133 SDRAM, systems based on th Intel® 845 chipset bring the performance advantages of the Intel® Pentium 4 processor to the high-volume mainstream PC market segment.

In addition to PC133 SDRAM, the Intel 845 chipset's memory controller hub (MCH) supports 1.5V AGP4X. The I/O controller hub (ICH2) supports PCI, 4 USB 1.1 ports, 2 ATA100 IDE connections, and 6-channel AC'97 audio, in addition to LAN and Lower Pin Count (LPC) interfaces. Intel® Hub Architecture provides a 1.8V, 8-bit/266-Mbyte/sec high-performance chip-to-chip interconnect.

While the maximum memory bandwidth of the Intel 845 chipset is 1.06 Gbytes/sec., it features a number of internal architectural improvements designed to optimize throughput and improve utilization of PC133 SDRAM memory:

- The Intel 845 MCH features a 256-bit-wide internal memory bus to optimize throughput.
- The in-order depth queue (IOQ) increases to 12 to match the processor and enhance the management of read requests.
- A 1,024-Kbyte write cache reduces latency.
- The MCH supports 24 open memory pages, that not only reduces latency, but also improves access during multitasking.
- Flexible memory refresh capability helps optimize available bandwidth by performing memory refresh during periods of lower memory activity.

Improved Board Designs

As bus speeds reach 400 MHz, reducing electrical noise becomes a significant issue for board designers. The process of simultaneously switching many signal lines can cause ground bounce, a form of crosstalk noise resulting from changes in current through the power and ground pins of circuits. The Intel 845 chipset introduces a Dynamic Bus Inversion (DBI) signal in each 16-bit data word that reduces simultaneous switching output (SSO) noise for improved signal integrity.

Other key board-level enhancements include:

- Full impedance and slew rate compensation, which mitigates board variations and environmental conditions.
- A 593-pin FC-BGA package for the MCH, which features on-package capacitors for improved power delivery to important interfaces.
- The new staggered ball array is designed for easier signal breakout and routing, which dramatically simplifies the design of 4-layer motherboards.

The mPGA478 Mechanical Reference Solution helps board designers cope with a number of thermal/mechanical and power issues:

- The Socket 478 design improves layout flexibility, with no fixed processor location required on the motherboard.
- Topside assembly eliminates the requirement for special tools during the assembly process.
- In addition to ensuring proper thermal performance and heat sink efficiency, the Heat Sink and Retention Mechanism for the processor and chipset provide board stiffening to help withstand shock and vibration during manufacturing and shipping.
- The new SFX12V power supply specification includes increased 12V DC current output for the Pentium 4 processor voltage regulator, in addition to increased 5V STBY current.The specified output is smaller on the SFX12V, which enables integration of smaller and more cost-effective power supplies. The SFX12V power supply specification is compatible with the current SFX1.1 specification.Intel is making several platform tools available so that developers can better evaluate their designs and decrease time-to-market. These tools include the Auto-Margining Tool and the Voltage Transient Test (VTT) Tool. Both are available from ADC Worldwide Tools and Technologies.

Summary

Systems based on the Intel Pentium 4 processor and the Intel 850 chipset meet the requirements of performance desktop PCs and entry-level workstations. The current challenge is how to extend the value of the Pentium 4 processor into the highly competitive and price-sensitive volume PC market segment. Cost-effective mainstream solutions require an optimized platform that can deliver the economy of PC133 SDRAM, with enhanced performance for current applications and headroom for the future.

Intel is helping OEMs and system integrators meet these demanding requirements with the Intel 845 chipset. In addition to an enhanced internal architecture that is highly optimized for the control of PC133 SDRAM, the chipset supports multiple board-level improvements. When used with the Intel's m478 Mechanical Reference Solution, boards based on the Intel 845 chipset can accelerate time-to-market development of high-volume mainstream PCs that deliver the value and performance of Intel's most advanced desktop processor.

More Info

For more information on the transition from PGA423 to mPGA478-based motherboard designs, see the article entitled Moving to Socket mPGA478 Desktop Boards in the September issue of *Intel Developer Update* magazine.

Visit the Intel Developer site for comprehensive design collateral including:

Pentium 4 processor:

- Intel® Pentium® 4 processor in the 478-pin package datasheet
- Intel® NetBurst™ Microarchitecture OS Writer's Guide

Intel 845 chipset

- Intel® 845 Chipset Product Brief
- Intel® 845 Chipset Sales Brief
- Intel® 845 Chipset Datasheet
- Intel® Pentium® 4 Processor in the 478-Pin Package and Intel® 845 Chipset Platform Design Guide (PDG)
- Intel® 845 Chipset Thermal and Mechanical Design Guideline
- Intel® 82801BA I/O Controller Hub 2 (ICH2) and Intel® 82801BAM I/O Controller Hub 2 (ICH2-M) Datasheet

For the latest information on test and design tools, e-mail ADC Worldwide Tools and Technologies.

Author Bio

Steve Bacchini joined Intel in 1984. Since then he has held various positions in product engineering and technical marketing for I/O components and now, chipsets. Steve currently manages Intel 845 chipset applications engineering team.

Departments

Desktop

Five Steps to Choosing the Right BIOS for your Desktop PC

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Overview

One of the least understood and most overlooked features of a desktop PC is the BIOS. Although the BIOS is a critical component of PCs, few developers think about the value a well-designed BIOS can add to a system. Instead, both developers and end users tend to think that a successful BIOS is one they never hear of and never have to deal with. The truth, however, is that the BIOS can make a significant difference in the overall quality of a PC system.

Most motherboard vendors get their BIOS from a major BIOS vendor. Although these BIOSes are usually fairly polished, they may not be as fully updated, automated, secure, configurable, or easy to use as one would expect.

Intel is one of the few motherboard vendors that build their own BIOSes. And, Intel® BIOSes are designed to be fully compatible with Intel® desktop boards and to take full advantage of the features of Intel® Architecture. Intel BIOSes include security features (such as fault-tolerant flashing), allow user-defined settings, and support a variety of other significant features. All developers should ask five key questions about the motherboards they're considering for purchase.

Five Key BIOS Questions

Before accepting a BIOS for a motherboard every developer should ask these five questions:

1. What kind of BIOS security is offered?
2. Does the BIOS ROM provide ample data storage?
3. Are warnings and error messages complete?
4. Is the setup utility user-friendly?
5. Can the BIOS handle special situations with the keyboard and mouse?

It's important for developers to be proactive about asking these five major questions because BIOS features are not otherwise likely to be disclosed. For example, many BIOSes don't have fault-tolerant flashing, digital signature technology, or error logging. Asking the questions early will help developers find out whether the BIOS they are choosing will provide the necessary security, will be easy to configure and use, and will be easy to recover during builds and system problems.

Security

Question 1: What kind of BIOS security is offered?

- Does the BIOS have fault-tolerant flashing of the boot block and other critical data?
- Is digital signature technology used to protect the BIOS from being flashed with rogue data?
- How many levels of access security are provided in the setup utility?

When the BIOS is not well protected, it can be flashed with rogue data or with another vendor's BIOS; it can be attacked and damaged by a virus, and so on. In other BIOSes, when something goes wrong during a flashing operation, the BIOS can be destroyed, thus reducing the PC to nothing more than a "boat anchor."

The Intel BIOS has extensive security features, including both fault-tolerant flashing and digital signature technology. Fault-tolerant flashing helps protect the BIOS in the event that the system is turned off or the power fails when flashing. Digital signature technology helps prevent the ROM from being flashed with the wrong vendor's BIOS or a virus. Digital signature technology also helps maintain the integrity of overall system security.

Data Storage

Question 2: Does the BIOS ROM provide ample data storage?

- Can developers incorporate their own OEM splash screen without creating a custom BIOS?
- Are multiple languages supported in the setup utility?
- Can users flash different languages into the BIOS?

Intel puts its BIOS on large firmware hubs to accommodate a richer feature set and give developers the option of customizing their systems. For example, with the Intel BIOS, developers can put their own splash screen into the BIOS.

Another benefit of ample data storage is the ability to support more than one language. The Intel BIOS includes ample storage space for up to five languages. For example, the Intel BIOS ships with five default languages: English, French, Italian, German, and Spanish. Users can flash in different languages as desired. (For information about language packages, contact your local Intel support representative.)

Ample storage space also allows for each Intel BIOS to contain a complete set of microcode updates for the processors it supports. This assures developers that all the right components are in each Intel BIOS flash package.

Errors

Question 3: Are warnings and error messages complete?

- Does the BIOS have error logging?
- Are there POST audibles?
- Does the BIOS have complete and up-to-date memory reporting?

Some motherboards still don't provide audible warnings before video is initialized. Some do not provide any form of POST error logging before or after video is initialized. In contrast, the Intel BIOS provides audible signals to indicate specific errors and warnings. Intel also provides full error logging in the flash memory, to help developers easily track and fix problems when building a system.

Setup

Question 4: Is the setup utility user-friendly?

- Is the setup utility easy to understand?
- Is the setup utility cluttered with legacy settings that are obsolete?
- Are there low-level performance settings that allow the end user to get into trouble?

Many of today's BIOSes include obsolete settings, outdated memory reporting, and other legacy issues. Terms like "extended memory" and "expanded memory" linger in many BIOSes, confusing end users and developers alike. This is an issue of end-product quality—whether the system is user-friendly or unfriendly, updated or outdated. A well-designed BIOS should be easy to understand and configure. The Intel BIOS has been designed to eliminate obsolete settings, outdated memory reporting, and obsolete language. It also automatically detects and configures certain settings.

Another shortcoming of many BIOSes is that they require users to change hardware settings that could otherwise be automatically configured. For example, some vendors require that the user manually turn on the UART2 Infrared feature in the BIOS. In contrast, the Intel BIOS detects and configures the same device automatically. This is both an ease-of-use and a support/cost issue. Users can get into trouble trying to change such obscure settings, and that can lead to increased support calls and system costs.

Keyboard and Mouse

Question 5: Can the BIOS handle special situations with the keyboard and mouse?

- Can the BIOS boot a swapped PS/2* keyboard and mouse?
- Does the BIOS support a headless boot?

Some systems still require PS/2 keyboard and mouse. However, PS/2 is not a hot-pluggable, intelligent bus. Plugging the keyboard and/or mouse into the wrong port is a nuisance that many end users would prefer to avoid. The Intel BIOS is designed to check for the keyboard and mouse, and it allows the boot to continue regardless where they are plugged in.

The Intel BIOS also lets the system do a headless boot (booting without keyboard, mouse, or monitor). Headless boots are both desired and/or necessary in some situations, such as in a server farm for a Web portal. A headless boot is a convenience to users, but it also helps expand the market for the PC, since the boards work in a variety of system configurations.

Five Additional BIOS Features

Aside from the five main features a well-designed BIOS should have, there are five secondary features that a good BIOS should also have.

These are the five secondary features:

- *10-second POST*. A system configuration with an optimized BIOS and well-selected components should POST in less than 10 seconds.
- *Custom BIOS defaults*. End users should be able to specify their own defaults without affecting factory-default settings. For example, the Intel BIOS allows users to configure system setup to their liking and then to save the configuration as their own custom default. The Intel BIOS saves the factory defaults separately from the custom default so that users can recover either configuration.
- *Minimal jumpers on the board*. With many BIOSes, there are unnecessary jumpers for configuring the system setup. With a well-designed BIOS developed in conjunction with the board, developers and end users can configure all settings through the setup utility. For example, Intel has only a single jumper on the board, and it's used for BIOS recovery. With an Intel BIOS, all settings can be configured through the setup utility.
- *Full support for WfM (Wired for Management) and boot-to-LAN*. This includes Boot Integrity Services (BIS) and a pre-boot execution environment (PXE). This also means that the System Management (SM) software is supplied with the proper SMBIOS info. The Intel BIOS fully supports both WfM and boot-to-LAN.
- *Windows* Hardware Quality Lab (WHQL) compliance for the advanced configuration power interface (ACPI).* Some BIOSes still allow the ACPI to be turned on or off, violating WHQL requirements. An Intel BIOS is fully WHQL compliant.

Although many BIOS vendors include one or more of these secondary features, it's rare to see all five features in a BIOS. The Intel BIOS is one of few that include all five secondary features, as well as the five main features.

More Info

Because clear, detailed descriptions are not usually available or easy to find for BIOSes, contact your technical support representative for more information about BIOS features, considerations, and comparisons.

Summary

Not all BIOSes are created equal. Rather, there is hidden value in the BIOS that developers may be overlooking. These benefits are not obvious—information about BIOSes is not easy to find through normal literature channels. However, getting some basic information about the BIOS can help developers buy the best motherboards for their needs.

Before deciding on a platform, ask the Five Questions about the BIOS for that platform. Security, data storage, error messages/logging, keyboards and mice, and system setup ease of use—information about these features will help indicate how poorly or well-designed the BIOS is. It may be unseen and it's usually ignored, but a well-designed BIOS can make a major difference in the overall quality of a desktop PC system.

Author Bio

Patrick Lang has been with Intel a year and a half as senior product marketing engineer in Intel's Desktop Products Solution Division. He has also worked in software development, software technical marketing, and software product management for the Intel® WebOutfitter℠ Service. Patrick received his B.S. in civil engineering from the University of South Carolina, and his M.S. in hydrology and water resources from the University of Arizona.

Integrators Can Cut Secondary Connectors—and Costs

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Overview

New software and hardware advances from Intel and third-party providers are helping to make ATAPI, WOL, and WOR connectors and cables obsolete in the desktop motherboard environment. This means that integrators, ROEMs, OEMs, and anyone else who configures and builds systems no longer must include up to five secondary connectors for supporting devices such as DVD players, CD-ROMs, LAN cards, and internal modems. Eliminating secondary connectors can yield a savings on purchase and installation of connectors and cables (see Figure 1) on hundreds or thousands of desktop motherboards. A corollary benefit is reduced complexity on the board and improved airflow for more robust operation.

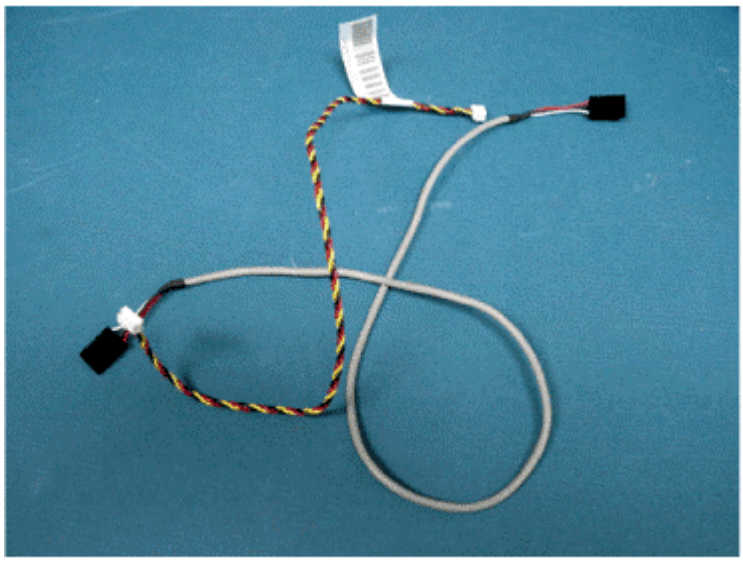

Figure 1. The grey cable is the analog audio cable and the twisted cable is the Wake on LAN cable.

To understand what these advances can mean for the development of systems based on Intel® desktop boards, consider the way integrators traditionally have implemented CD audio, telephony, Wake on LAN, and Wake on Ring technologies. Then consider how they can implement such features without the need for secondary connectors or cabling.

ATAPI CD-ROM and ATAPI AUX

These connectors, black and beige respectively, are generally located near the integrated audio component. They measure about a half-inch across (see Figure 2) and thus consume a fair volume of board real estate. ATAPI CD-ROM and ATAPI AUX are used to send an analog audio signal from a CD-ROM, DVD-ROM, or CD-R/RW device, with ATAPI AUX also supporting the case of two devices in a single system needing to transmit analog audio signals simultaneously. With either connector, the device reads the digital media and converts the data to an analog signal with some loss of signal quality.

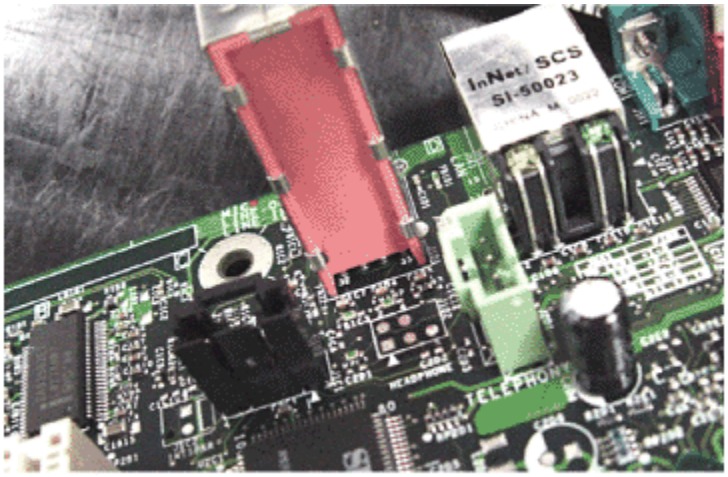

Figure 2. The ATAPI CD-ROM connector, which consumes significant space on the board, becomes unneccessary when the operating system supports digital audio over the IDE channel.

Recently, popular operating systems have begun to support digital audio over the IDE channel. In this arrangement, the device reads the digital media and sends the data directly over the IDE channel to the audio component. Next, the audio component converts the signal to analog and sends it to the speakers. There is less loss of signal quality with the conversion performed by the audio circuitry, since it is usually equipped with high-sampling DACs and is exposed to comparatively low levels of EMI.

Microsoft Windows* 98SE, Windows Me*, Windows 2000*, and Windows XP* support this technology natively and by default. Consequently, integrators building systems designed to function in any of these operating-system environments do not need ATAPI CD-ROM or ATAPI AUX connectors or corresponding cables.

ATAPI Telephony

This connector is green in color and, like ATAPI CD-ROM and ATAPI AUX, about a half-inch across. It is used to send voice data in analog format from an internal modem to an audio component. Now, however, many PCI modems are capable of sending voice data through the PCI bus to the audio component in digital format. If the modem that you integrate supports digital voice then the ATAPI Telephony connector and cable are not necessary.

WOL (Wake on LAN)

This is a three-pin connector that cables directly from the motherboard to a LAN device and enables that device to "wake up" a system from the ACPI S1 and S3 states. Most LAN devices support waking from S1 or S3 through a Power Management Event (PME) signal. Such devices can be inserted into a motherboard PCI or CNR slot that contains PME signal circuitry. For example, the Intel® LAN device is routinely sold in the LAN on Motherboard (LOM) form and includes WOL circuitry.

This approach means that on Intel desktop boards, integrators no longer need a WOL connector with a LOM SKU. It means also that on an SKU with an Intel LAN card inserted into the CNR or PCI slot integrators can forgo WOL connectors and cabling with no loss of functionality. The Intel desktop board enables PME signals to the CNR connector and the PCI slot closest to the AGP.

WOR (Wake on Ring)

This is a three-pin connector that enables a modem to send a signal to the motherboard and wake a system from ACPI state S1 or S3. Most modems support wake via PME. This means integrators building a system with an internal CNR or PCI modem that supports this technology can integrate the modem into the CNR slot or the PME-enabled PCI slot on an Intel desktop board without the need for a WOR connector or cabling.

Summary
A number of software and hardware technologies are enabling integrators to incorporate advanced audio, video, telephony, and other capabilities directly on the motherboard without the need for secondary connectors or cabling. These technologies include operating-system support for digital audio over the IDE channel, modems capable of sending voice data to the audio component in digital format, and LAN and modem devices that support PME signaling through the PCI bus.

As a result, integrators, ROEMs, OEMs, and anyone else who configures and builds systems based on Intel desktop boards or other motherboards can save money on parts and labor while reducing complexity and crowding on the board. Additional benefits include an overall lower system cost and improved airflow for cooler and more robust operation with equivalent or enhanced functionality.

More Info
For more information on digital audio operating system support, go to the Microsoft Driver and Hardware Development Web site.

Author Bio
Michael Cofield is a technical marketing engineer in the Intel Architecture Marketing Group. He has served as part of the team responsible for launching an Intel desktop board based on the Intel® Pentium® 4 processor and using DDR SDRAM technology. Michael holds a B.S.E.E. from Santa Clara University and is a member of IEEE and USB-IF.

Initiatives and Technologies

Extensible Firmware Interface (EFI): Changing the Way You Look at BIOS

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Performance Tools Operation
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Overview

Just as the PC revolutionized the computing world 20 years ago, system software based on the Extensible Firmware Interface (EFI) specification may permanently change the way Intel® Architecture-based computers are designed. The EFI specification defines a new model for the interface between operating systems and platform firmware. The interface consists of data tables that contain platform-related information, plus boot and runtime service calls that are available to the operating system and its loader. Together, these provide a standard environment for booting an operating system and running pre-boot applications (see Figure 1).

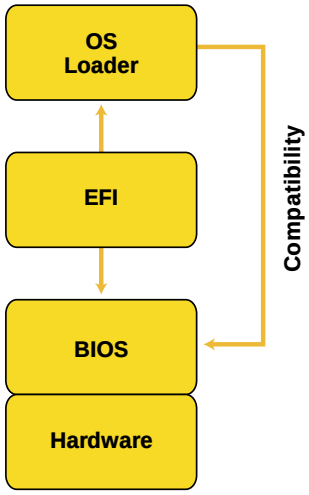

Figure 1. How EFI fits in with BIOS and overall system design

Features and Benefits of EFI

EFI provides clear advantages for system designers, manufacturing test application developers, system administrators, and OEMs. Because the EFI API reduces the need to address compatibility and maintenance issues encountered with legacy firmware, it can shorten development and testing cycles and ultimately, speed time-to-market. Features and benefits of EFI include:

- Allows EFI driver code to be written in C. Writing EFI drivers in C rather than assembly code benefits the developer in many ways, one example being the ability to simply and easily reuse code between drivers.
- Provides a standardized driver model. Given the driver model described in the EFI specification, a hardware device such as a PC-AT keyboard can be replaced with a USB keyboard without requiring changes in applications such as OS loaders or test applications, as long as the EFI API is used. Before EFI, painful legacy BIOS changes and operating system changes could have been required for such a change.

- Offers a pre-OS landing point. Since the EFI shell provides a pre-OS execution environment, OS-independent tools can be created, allowing system configuration and testing *before* the operating system is installed or running.
- Provides support for a legacy-free environment. Drivers interface with EFI directly through an API defined in the EFI specification.
- Supported currently by 64-bit Intel® Architecture-compatible operating systems such as Windows XP*, Linux for Itanium™ processors, HP-UX*, and AIX* 5L. EFI is supported by 32-bit Linux* as well.
- Offers extensive pre-boot system functionality such as remote console redirection, allowing remote systems administration.

Looking Ahead

EFI may indeed become the *one* way to boot up computers in the future. Next-generation IA-32 processor-based computers are expected to incorporate EFI in their system designs. Soon to be released, the EFI specification 1.1 offers modular option ROM drivers, which will make it easier for system developers, and add-in card vendors in particular, to include EFI in their system design. Developers are already incorporating EFI into set-top boxes and considering EFI for handheld devices.

Summary

Get ready for the next generation of IA-32 and Itanium processor-based systems. Explore the opportunities to cut your time-to-market, develop a legacy-free environment, and experience pre-OS functionality. Download the EFI specification, easily modified sample code, application tool kit, and EFI core from the Intel Web site. Start incorporating EFI into your own system design and send Intel your feedback (through the EFI Web site). You may find the opportunities are boundless.

More Info

To learn more about EFI, visit the EFI section of the Intel Web site and download the EFI specification and sample code, including the application tool kit.

Author Bios

Mark Doran manages the team that developed the Extensible Firmware Interface (EFI) specification for Intel® Architecture systems. This team also helped to develop the System Abstraction Layer (SAL) specification and reference implementation for the Intel® Itanium Architecture. Currently, he is working on enabling rollout of the EFI specification version 1.1 designed to replace legacy option ROMs and developing infrastructure to support the move of EFI into IA-32 processor-based systems.

Paul Parenteau joined Intel Corporation after 11 years with Sequent Computer Systems. He currently manages the VTune™ Technical Marketing Engineering team and was previously the manager of the EFI/Tiano Technical Marketing team. Much of his background is in engineering of high-end symmetric multiprocessing (SMP) server systems running the UNIX* operating system. He holds a B.S. degree in computer science from the Oregon State University.

Networking & Communications

New Network Processors for Next-Generation Networks

Nick Finamore
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Network Processor Business Unit
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Overview

Next-Generation Network (NGN) technology will carry data, voice, and video with equal effectiveness while providing the performance needed to support the rollout of new bandwidth-intensive services including distributed content and broadcast-quality video. Within this emerging NGN environment, the value of network processors in customer premises equipment (CPE), network access/edge devices, and core/metro applications will depend on their level of service intelligence.

While the core speed of the NGN infrastructure is evolving to 10 Gbps and beyond, the ability to flexibly and affordably provision multiple network services is enormously important to carriers and service providers. In this new world, traditional “feeds and speeds” no longer provide an adequate measure of overall network processor value. Instead, the key will be the amount of intelligence, defined as the amount of processing capacity devoted to deep packet inspection that these processors can apply during the short life of a packet. At OC-192 for example, the arrival rate of a 40-byte IP packet is a mere 35 nanoseconds.

While network processors are at the heart of networking equipment designed to enable new services, it is unrealistic to expect a single network processor, or even a single family of processors, to cost-effectively meet all of the specialized and varied application requirements of the CPE, access/edge, and core/metro market segments.

The industry needs more flexible choices than either ASICs or present-day network processors can provide. To deliver these choices, Intel is developing three new network processor families specifically optimized to meet the unique application requirements from CPE, to access/edge, and the metro area network (MAN) and network core. Intel’s new low-power, flexible, high-performance network processors are designed to meet the special requirements of NGN applications at multiple bandwidth and cost points, while providing headroom for upgrades and ongoing product differentiation.

Developers who are familiar with the flexibility and reliability of the Intel® IXP1200 Network Processor family will see these capabilities dramatically extend to encompass fully programmable network processor architectures capable of scaling to 10 Gbps and beyond.

Technology Drivers

Figure 1 illustrates the three NGN market segments: CPE, access/edge, and core/metro, and lists some of the primary applications within each segment.

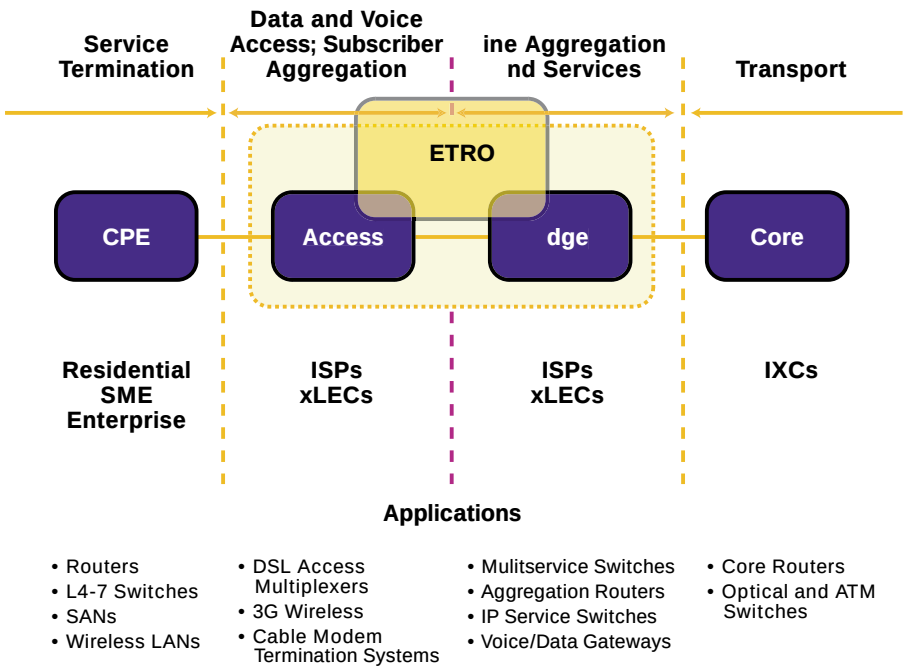

Figure 1. The unique network processing requirements of network and application segments

CPE devices must meet a wide variety of requirements. These include wire-speed performance on the WAN, and interoperability with access equipment at Layers 1 and 2, and with edge equipment at Layer 3. In addition, CPE needs to support a variety of protocols and permit easy configuration and remote management by the service provider. Devices should provide the headroom to support emerging standards and performance upgrades, and do all of this at low cost.

Access devices provide data and voice aggregation, while edge devices provide line aggregation and services provisioning. Devices at the network edge deliver differentiated network services based on traffic characteristics. High-performance routing switches are used to enforce network management policies, categorize traffic flows, allocate bandwidth, set queuing priorities, and make optimized route determinations.

At the core, high-bandwidth systems aggregate and move traffic from hundreds of edge devices using multi-gigabit and terabit switching fabrics. Equipment implemented at the network core will increasingly require direct connectivity to Dense Wave Division Multiplexing (DWDM) optical infrastructure as ATM-based networks give way to IP-over-fiber based configurations.

Three New Processor Families

Intel plans to introduce three second-generation processor families tailored to the unique characteristics of the CPE, access/edge, and core/metro market segments. These three new network processor families will share key architectural attributes, including flexibility, scalable performance as well as tight functional integration between control and data planes. The variety of processor families will enable developers to choose the network processor building block best matched to the price/performance requirements of their applications. In addition, a common tool suite will minimize customers' training and support costs, and facilitate reuse of code across processors.

One critical challenge for network equipment hardware designers is how to provide adequate processing headroom to quickly support new services and applications for fast time-to-market development, while keeping costs as low as possible. Intel's next generation technology enables faster deployment of intelligent network services by combining high performance processing with unlimited programming flexibility and code re-use. Scalable microengines provide support for a broad range of line speeds, currently ranging from OC3 to OC192. High performance and scalability is achieved through a multi-threaded distributed cache architecture and pipelining features in software. The microengines feature innovative inter-thread communication capabilities for efficient processing at high line rates and general-purpose hardware elements that enable advanced networking algorithms and rich network processing in converged communications environments.

Intel® network processors meet this challenge three ways. The first is through advanced multiprocessing techniques with multiple multithreaded microengines that perform data-plane processing required for deep packet analysis. Intel has further enhanced this parallel architecture with a combination of software pipelining with low-overhead inter-process communications. Finally, Intel network processors feature a distributed caching architecture that puts memory resources where they can be most efficiently used by the microengines while reducing memory latency.

Intel's network processing architecture implements tight logical and physical integration between control-plane and data-plane components to minimize processing latencies and component integration costs. In addition to the microengines, Intel network processors also share a low-power, high-performance Intel® XScale™ microarchitecture core for robust control-plane functions including packet exception handling and route table management. Intel XScale technology delivers industry-leading MIPS/mWATT performance while providing effective heat dissipation for space-constrained form factors such as rack-mounted blades and access/edge devices.

Overall, the combination of multiple, tightly integrated processing elements, heavily pipelined packet processing, and distributed caching provides the processing headroom needed for tomorrow's rich services and faster line rates. The fully programmable store-and-forward architecture of Intel's network processors will enable customers to flexibly and rapidly develop, modify, and control the wide range of software needed to differentiate their products, including flexible Quality of Service (QoS) algorithms and emerging communications protocols. Re-usable code makes it a relatively easy matter to modify software to introduce innovative features and stay a step ahead of the competition.

Enabling Emerging Applications

Intel's next-generation network processor roadmap focuses on meeting the requirements of four of the fastest growing application segments. Each of them makes unique demands on the network processor.

Broadband Access Devices

Broadband access equipment includes a wide range of xDSL, cable access, and passive optical networking equipment including fiber-to-everywhere in the access loop. At the CPE end of the broadband market segment, multiple protocol support and cost minimization are absolute essentials. Intel will meet these requirements with a specialized family of highly integrated, programmable, and cost-optimized network processors.

Consolidating traffic from multiple customer premises to the network core requires large-scale and cost-effective aggregation of multiple low-speed connections to higher speed traffic at successively higher levels of the network. Here port density and real estate requirements are critically important. Access equipment increasingly features a variety of different blades in a single chassis, so network processors need to support multiple protocols and standards from point-to-point protocol (PPP) to the Data Over Cable Service Interface Specification (DOCSIS). As new protocols and standards emerge, traditional ASIC-based designs simply do not provide the needed flexibility.

Because line rates in broadband equipment are generally less than OC-48, the challenge for developers is to balance MIPS performance and cost for today's applications, with the performance headroom needed for future innovations. Intel's next-generation network processor family will provide badly needed choices. They will make it possible for developers to combine the right mix of performance scalability with deep packet inspection for such functions as IP classification, billing, traffic management, and remote management, while helping to meet power and cost requirements for high port density.

Multi-Service Switches

Multi-service switches (MSS) are places where multiple data types, including voice, converge at the edge of the network, and where rich service provisioning takes place. At the same time, devices must support increasingly faster line rates, including OC-192 uplinks to the network core. The engineering challenge is how to combine wire-speed performance with the deep packet inspection required for an ever-growing array of rich converged services.

On the downstream side, MSS devices need to support Voice over Packet capability, virtual LAN functionality, packet classification, traffic management, IP QoS, security, and a host of differentiated IP services to individual subscribers. This equipment also needs the ability to perform protocol conversion, enable emerging routing standards such as multi-protocol label switching (MPLS), and support the emerging IPv6 protocol for address management and security.

The need to quickly implement multiple emerging protocols makes programmability extremely important, and the deployment rate of new services allows no time to spin a new ASIC. The challenge is how to provide these rich services at a line rate of 2.5 Gbps and beyond. In ASIC-based designs, the answer can involve compromising available feature sets in an attempt to maintain acceptable line-rate performance.

Intel's next-generation network processors will provide fast and scalable processing performance with abundant headroom. Their programmability means that developers will no longer find themselves making trade-offs between performance and reduced services, as required with ASIC-based designs.

Wireless Infrastructure Applications

The wireless infrastructure is a world unto itself. The emergence of new wireless standards, including 2.5G and 3G, is underway. As to the exact timing, no one can really say. What is clear is that wireless represents one of today's fastest-growing application segments. A recent market analysis reported that by the year 2006, the number of wireless connections will surpass the number of landline connections. (Source: *Wireless Infrastructure Technology and Marketing: Evolution to 2.5G and 3G*, by James E. Gunn, published by Forward Concepts, 2000).

Equipment in this segment ranges from relatively simple low-speed base station transceivers (BTS) to base station controllers (BSC) that aggregate traffic from transceivers and move it at OC-192 rates. Other applications include radio network controllers, Gateway General Packet Radio Service Support Nodes (GGSN), Service General Packet Radio Service Support Nodes (SGSN).

Network processors must be capable of supporting lower-cost and extended-temperature operation for BTS devices, high line rates for BSC and SGSN applications, and support a wide range of services such as IPv6, AAL2 segmentation and reassembly, MPLS, and IP QoS functionality.

By providing a wide range of performance and feature options, Intel's new network processors will enable the industry to balance performance, extended temperature capability, and cost with the programmability and software portability needed to develop new generations of wireless products.

Core/Metro

The three requirements for this application segment are performance, performance, and even more performance. To handle the dense wave division multiplexing (DWDM) requirements of the metro area network (MAN) and core SONET/SDH applications, including core switches and multi-Gigabit routers, the network processor must be capable of performing deep packet inspection at 10 Gbps and beyond. As in other application segments, headroom for even faster line rates is essential.

The core represents a challenging new application space for network processors, and the selection of the right components is an absolutely critical decision. In addition to extremely high performance, network processors used at the core must support a variety of specialized circuitry and features to support the spectrum of 10 Gbps, DWDM, and ATM connections.

Intel has solved the technical chip design issues required to move network processor performance to 10 Gbps and even faster line rates and provided public illustrations of its next-generation technology performing packet inspection in 35 nanoseconds. Intel's core competency in silicon process technology and integration is enabling rapid evolution of network processor performance.

Tools to Speed Development

As with its first-generation IXP1200 Network Processors, Intel will offer a robust suite of software and hardware development tools to decrease time-to-market and minimize development costs for customers. The comprehensive software development environment includes a cycle-accurate simulator for the new, high-performance network processors, enabling rapid implementation of rich services. The recent Intel Developer Forum Conference (IDF) Fall 2001 included a public demonstration of the simulator, highlighting Intel's ability to support customers' development efforts in advance of silicon availability.

Intel will also provide flexible, chassis-based hardware development platforms to enable configuration, testing, and debugging of a broad range of application environments. Intel will maintain the "look and feel" of its current development platform, ensuring an easy-to-use graphical interface, and minimizing training and support costs.

Summary

Intel is committed to accelerating the industry's ability to deliver next-generation services. In the near term, Intel will significantly expand its network processor offerings with the introduction of three new network processor families designed to meet the respective requirements of CPE, Access/Edge, and Core/Metro market segments.

As performance and processing requirements continue to diversify for each segment of the network, it is increasingly unlikely that a "one size fits all" approach to network processing can deliver a balanced mix of service-aware packet analysis and cost. Three families of network processors, each optimized to the characteristics of a given segment of the network, holds the greatest promise for the NGN.

With a wide range of price/performance-optimized network processor families to choose from, and the added advantage of programmability and software portability, the industry will be able to offer customers the best combination of flexible multi-service provisioning capabilities and wire-speed performance while minimizing development time and costs.

More info

Additional information regarding Intel's network processor roadmap is available for developers. This information is Intel Confidential and is available under Non-disclosure Agreement. Contact your Intel representative for details.

Download the white paper by clicking on the Highlight *Intel Defines Next Generation Network Processing* on the Intel® Developer Web site.

Author Bio

Nick Finamore is the general manager of the Network Processor Business Unit, based in Hudson, Massachusetts. His group is responsible for network processor solutions for access, edge, and core/metro applications.

Nick joined Intel in 1985. Since then he has held a variety of sales, sales management, and applications engineering management positions. Nick earned his B.S.E.E. at Cornell University.

Servers

Intel® Xscale™ Microarchitecture Development Tools

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Overview

The Intel® XScale™ microarchitecture is optimized for low power consumption and high-performance processing in market segments ranging from battery-powered, wireless, and handheld applications such as digital phones and personal digital assistants to Internet infrastructure applications including network processors and intelligent I/O processors.

To complement the introduction of the Intel® 80200 processor with XScale microarchitecture, Intel and a growing list of third-party vendors now provide a comprehensive development tools environment designed to jump-start the development process for next-generation products.

The Intel XScale microarchitecture development environment features evaluation boards and hardware designs in addition to software development suites that can get application development off to a fast start. Other tools building blocks include real-time operating systems (RTOS) and associated development tools, specialized companion chips and field-programmable gate arrays (FPGAs), JTAG and debug tools, a logic analyzer, and various software models.

This growing tools environment provides many of the building blocks you can use to keep your XScale microarchitecture development program ahead of the curve, freeing you to concentrate your engineering resources on value-added functionality.

A comprehensive summary of available tools is now listed on the Intel developer Web site along with links to third-party tools vendors.

Intel® IQ80310 Evaluation Platform

The Intel® IQ80310 Evaluation Platform, based on the Intel® IOP310 I/O processor chipset, is a low-cost kit designed to enable the rapid development of I/O software for intelligent Internet storage and RAID applications.

The evaluation platform provides a comprehensive solution for rapid software development in convenient kit form. It provides support for hardware and software debugging with JTAG, Ethernet, and serial ports, and even has MICTOR connectors for a logic analyzer connection.

Contents of the kit include:

- Cyclone Microsystems* IQ80310 PCI board
- Core development tools—ARM ADS v1.1* CD-ROM (Evaluation Copy) and Cygnus/Red Hat GNUPro CD-ROM
- Software images for supported real-time operating systems and debug monitors—Wind River Tornado development environment CD-ROMs (Evaluation Copies), LynuxWorks BlueCat* CD-ROM (Evaluation Copies), and a flash recovery utility CD-ROM
- Electronic manuals and documentation

For details visit the Intel IQ80310 Web site.

Reference Platforms

A variety of reference designs are currently available from third-party vendors. Visit the Intel XScale Microarchitecture Tools Web site regularly for the latest updates.

- *The ADI Engineering 80200 EVB* reference platform* is designed for a broad range of applications based on the Intel 80200 processor with XScale microarchitecture and includes a FPGA chip for use in communications applications.
- *Wind River Systems* provides the Intel XScale 80310 PPMC* and the Tornado for Intelligent Network Acceleration (TINA) Development Platform*. The TINA platform is designed to speed the development of TCP/IP offload applications using the Intel 80200 XScale microarchitecture core processor. The PPMC board is designed for a broad range of applications based on the Intel® 80310 I/O processor chipset.
- *The Team ASA NPWR* platform* is a reference design for network attached storage (NAS) controllers, RAID controllers, Linux* servers, and Internet server applications.

Tool Chains

To simplify transitional development from earlier RISC processor-based designs, the i960® C-Tools user environment has been ported to the Red Hat GNUPro* compiler. The compiler, assembler, and linker support specific optimizations for the Intel XScale microarchitecture, the ARM instruction set v.5TE, and Intel® DSP extensions.

Red Hat GNUPro 2000* Tools include:

- gcc C Compiler, g++ C++ Compiler, gdb/Insight Debugger, Source Navigator IDE
- RedBoot* Debug Monitor & Bootstrap Solution
- GNUPro 2000 Tools on the Intel Web site
- GNUPro Tools for XScale on the Red Hat Web site

ARM Developer Suite (ADS) Tools* include:

- ARM & Thumb* C & Embedded C++ Compiler, CodeWarrior IDE, AXD Debugger
- ARMulator Instruction Set Simulator
- ARM Firmware Suite (AFS)—Angel Debug Monitor

RTOS and Tools

A wide variety of real-time operating systems and tools are currently available from leading vendors.

The following list is a summary of available solutions. Check the Intel XScale Microarchitecture Tools Web site regularly for the latest information.

RTOS solutions:

- Accelerated Technology Nucleus*
- Enea OSE*
- Express Logic ThreadX*
- LynuxWorks BlueCat
- Microware OS-9*
- Monta Vista Hard Hat Linux
- Wind River IxWorks* and VxWorks*

JTAG and debug tools:

- ARM Multi-ICE*
- EPI MAJIC*
- Macraigor Systems Raven*
- Sophia Systems
- Wind River visionPROBE*

Debugger:

- Wind River visionCLICK*

Models:

- ARM ARMulator*
- Red Hat Instruction Set Simulator (ISS)*
- VaST Systems Co-Design Model*

Companion chips:

- ADI Engineering/Xilinx FPGA Memory Controller
- Intel® 80312 Companion Chip for RAID applications

Logic Analyzer:
The Corelis Logic Analyzer Probes for the Agilent family of logic analyzers provides access to all signals for the Intel 80200 processor. It enables the connection of a target board to the logic analyzer for timing and state analysis.

Summary

Numerous development tools for the Intel XScale microarchitecture are now available from Intel and leading third-party vendors to speed the development of intelligent Internet storage, networking, communications, and handheld applications and devices.

This growing tools environment includes hardware reference platforms, companion chips, robust software development suites, real-time operating systems, debuggers, JTAG and debug tools, logic analyzers, and models. Available tool chains include compilers, assemblers and linkers that support specific optimizations for the Intel XScale microarchitecture, the ARM instruction set v.5TE, and Intel DSP extensions.

The Intel XScale microarchitecture tools environment provides a launch pad for the development of low-power and high-performance products across a wide range of Internet applications.

More Info

For a comprehensive summary of available tools and links to third-party vendors, visit these areas of the Intel Developer site:

- Intel IOP310 Third-Party Development Tools
- Intel IQ80310 Development Board and available sample code
- Intel XScale Microarchitecture Technical Summary
- Intel® Intelligent Internet Storage Building Blocks

Author Bio

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Migration to the Next-Generation Contact Center

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Overview

The increasing convergence of voice and data (or telephony and computers) has fueled a demand for multifunctional, multimedia, and fully integrated contact center solutions based on VoIP (Voice over Internet Protocol). Businesses rightly see these solutions as a way to reduce operational cost, increase customer satisfaction, expand their market reach, and enhance their ability to establish distributed contact center operations—all while protecting their investments in core business applications. In response, application service providers, VARs, system integrators, telecom equipment manufacturers (TEMs), and ISVs are working to provide contact centers with VoIP networks that are integrated with business applications and legacy switching environments as well as with speech technologies and cross-media communications.

The foundation of such networks is IP telephony, which converts an analog voice signal to a digital signal so it can be sent over an IP network. IP telephony may be known better in the consumer arena than in the contact center, as the technology has been available to Web users as a “free” option for long-distance calling since the mid-1990s. But wide-scale consumer adoption has been hindered by poor voice quality and the fact that consumers had to be in front of a PC to use the service.

Corporate contact centers have had their own reasons for delay in adopting IP telephony on a large scale. In addition to voice quality issues, advanced features such as hold, retrieve, park, pickup, transfer, and multiparty conferencing—all widely used in contact centers—were long available only in circuit-switched telephony environments.

What’s different now is that solution developers have access to these advanced features for VoIP technology, and can build a full-featured VoIP-based contact center that offers excellent voice quality. Contact centers can migrate smoothly to such an environment without sacrificing features or functionality. This means they can enjoy the advantages of VoIP while retaining current business applications such as workforce scheduling, screen pop, and customer records updating.

Building Blocks Speed Development

Adding VoIP elements to contact center solutions has been a challenge for developers, largely because they have lacked experience with VoIP technologies. But now, Intel (among others) is making available standards-based hardware and software "building blocks" based on Intel® Architecture. The hardware building blocks include:

- Media-processing components for voice, fax, and speech
- Appliances for connecting network-hosted voice applications
- PBX integration boards, line tap boards, and IP telephony boards
- Platforms supporting applications, peripherals, and service from multiple vendors on a single system

The software building blocks from Intel include:

- Core components for linking applications and switching environments
- Programming interfaces for integrating calling features into Web-based business applications
- A queuing system
- Modules supporting interactive voice response integration and routing
- Assorted tools for development and testing

Consulting services also are part of the Intel offering to developers working on VoIP-based contact center solutions. These services address the full solution life cycle, from planning and design to implementation and maintenance.

The Simplicity of a Unified Infrastructure

The Intel® VoIP building blocks for a typical contact center include a Media Gateway Server, Media Gateway Controller with third-party call control, IP Media Server, Universal Queue Server, and Call Processing Server. These products are designed to deliver features traditionally provided by the PBX, ACDU (automatic call distribution unit), and IVR (interactive voice response). The Intel VoIP client, which is a software component running on a client PC or customer-support Web site, can eliminate the need for an expensive full-featured phone at the desk.

With these building blocks, developers can build a VoIP-based contact center with a vastly simplified infrastructure. For example, a single network line can provide each desk with voice, data, supplementary services, and conferencing. Ultimately, a VoIP-based contact center can move to a single unified network infrastructure, dramatically reducing wiring, equipment, and support costs.

In the meantime, many contact centers that are based on PSTN and circuit-switched telephony will be migrated to VoIP in a way that retains their traditional PBX solutions while adding VoIP capabilities solutions in selected segments of their operation. As VoIP-based solutions are proven, the contact center may eventually migrate to a fully VoIP-based environment, realizing the full benefits of a single network infrastructure for voice and data.

Other products from Intel, namely the Computer Telephony (CT) building blocks such as CT Connect, can ease the transition from PBX to IP switching environments.

Summary

A growing number of application service providers, VARs, system integrators, TEMs, and ISVs are seeking to launch or expand VoIP-based contact center solutions. This is because the availability of excellent voice quality and advanced call-management features is fueling the interest of their enterprise and service provider customers in new VoIP capabilities. Evaluating IP telephony building blocks from Intel is a good place for such developers to start.

More Info

More information on two of the Intel® IP telephony building blocks, the Intel® Internet Phone SDK and the Intel® CSTA Gatekeeper, is available at the Intel® Communication Systems Products area of the Intel Developer Site.

More information on Intel Consulting Services is also available from the site.

In addition, the site offers technical detail on VoIP solutions and building-block technology, and code samples.

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Web Development

Standards for Process Coordination Technology Move Toward B2B Automation

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Overview

Online commerce has yielded significant cost reductions for vendors, but less so for buyers. This is beginning to change, thanks to the increasing adoption of XML-based B2B (business-to-business) process coordination technology (PCT), which promises online buyers easier access to an assortment of standardized B2B processes enabled by workflow modeling technologies. But there is still a long way to go. This is because for many developers, the lack of uniform and consistent industry standards makes developing and implementing PCT solutions prohibitively expensive.

To address this challenge, Intel is working closely with industry groups that are promoting standards for richer functionality such as process description, negotiations, and transaction support. Such groups also are working on a convergence of standards. With this convergence, the best aspects of diverse and potentially conflicting standards will be brought together in a manageable, complementary, and non-overlapping set (see Figure 1). Intel is also working toward ensuring that the software implementations of these standards will take advantage of Intel® Architecture platform capabilities in the areas of quality of service, security, and encoding to name a few.

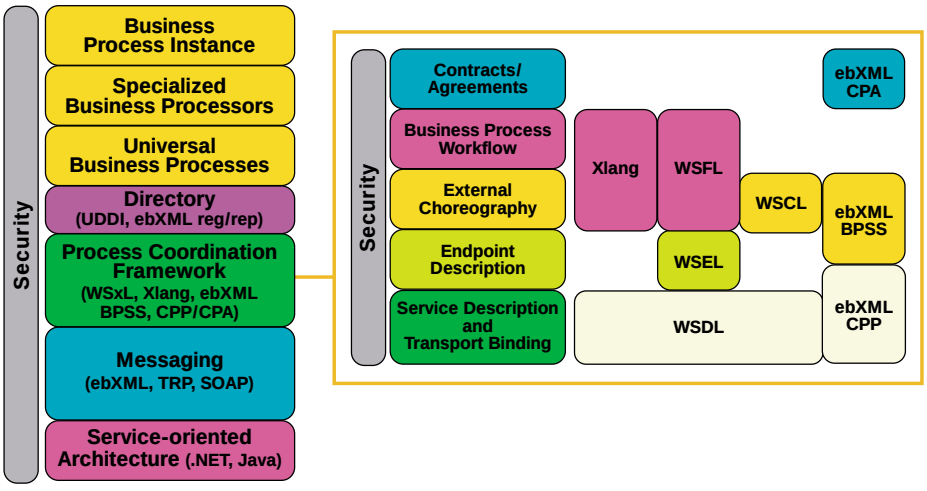

Figure 1. Process coordination technology (PCT) standards are a key part of industry efforts to futher automate B2B transactions. In each "solution stack" the higher layers build on the functionality of the lower layers.

The ultimate goal of both endeavors is to give corporate developers and ISVs enhanced communication capabilities with business analysts and greater access to automated code generation and code that is robust, reusable, and interoperable.

Current Technologies

Before reviewing the current crop of PCT standards, consider the requirements to which these specifications are intended to apply. Prominent among them are the technologies listed here, now available for Web services process workflow, business process modeling, and related B2B activities:

Service descriptions and transport bindings enable the description of operations that can be invoked on the Web service, messages exchanged during the operation, and protocol bindings (e.g., for HTTP or SMTP). Service descriptions are meta-level descriptions of a service in terms of its operations. Transport bindings tie such operations to specific physical addresses of the service providers.

Endpoint descriptions enable the description of additional service-endpoint or operation properties such as quality of service.

External choreography enables the description of the order in which external users of a Web service will invoke its operations. Such a description includes legal ordering of the operations supported by the Web service.

Business process workflow defines the internal execution of a sequence of functions that constitute a Web service, also known as a well-defined flow of operations, to fulfill a business need.

Contracts use an XML-based syntax to define the agreement under which two entities will conduct e-Business.

Security defines the various levels of security that may be required at their respective layers of the PCT stack Security comprises authorization, authentication, confidentiality, and non-repudiation.

Current Standards and Specifications

Intel is actively participating in groups such as CPP/A and the Business Internet Consortium Initiative for a formal approach to enhancement and convergence of the standards that apply to PCT and the specifications defining them. Here are the most prominent among them:

WSDL (Web Services Description Language). Submitted to the World Wide Web consortium (W3C) by Ariba, IBM, and Microsoft, WSDL is an XML-based specification describing a Web service as a set of endpoints. Through this description, WSDL provides a way to bind operations and messages to concrete network protocols such as HTTP and SMTP.

WSCL (Web Service Conversation Language). Developed by Hewlett-Packard, WSCL is an XML-based specification for defining conversations and the ordering of messages exchanged between parties on the Internet. Layered on top of WSDL and ultimately to be incorporated into it, WSCL focuses on specifying the sequence in which operations can be invoked.

WSFL (Web Services Flow Language). Developed by IBM, WSFL is an XML-based specification for describing process workflow and Web service compositions. Layered on top of WSDL, WSFL defines two kinds of Web service compositions: flow model, describing the structure of the business process, and global model, describing how composed Web services interact with one other.

WSEL (Web Services Endpoint Language). The IBM WSFL documentation refers to a standard for an endpoint language. Note that the requirements to which this specification would apply is still in progress, but it likely will specify information on cost, regional specialization, transport and operational guarantees, and physical location.

ebXML (Electronic Business XML Initiative). ebXML, a set of specifications sponsored by the United Nations and OASIS to enable an electronic business framework, is the richest of all the specifications discussed in this article. ebXML has some notion of security and endpoint description and, in contrast to the service-interface focus of WSDL, is strongly focused on B2B.

XLANG (XML Language Business Process Description). Developed by Microsoft, XLANG is an XML-based specification for describing a workflow or implementation of an e-Business service, depicting actions and sequencing. Layered on top of WSDL, XLANG builds on the process-description XML code generated by the Microsoft BizTalk* Server Orchestration (a Visio*-based graphical modeling tool).

Summary

Having rich XML-based B2B process coordination technology (PCT) solutions will dramatically help businesses to reap the cost advantages of online commerce, especially in their capacity as buyers. But for such solutions to become widely available, corporate developers and ISVs must have an easily manageable set of standards and specifications to follow.

For this reason, Intel is working closely with industry groups whose goals are twofold: first, to converge the strongest aspects of existing standards into a manageable, complementary, and non-overlapping set, and second, to promote the enhancement of standards to take advantage of the Intel Architecture platform environment. Intel and other industry leaders hope that in the long run this work will lead to a single specification addressing all the features and requirements necessary for the cost-effective implementation of powerful PCT solutions.

More Info

To learn more about two industry groups that are working, respectively, to enhance and converge standards for PCT solution development and to develop standards and specification for XML interoperability in general, visit the Internet Business Consortium and OASIS Web sites.

Author Bios

Tim Collier is a staff software engineer in the Intel e-Business Solutions Lab. He serves as an Intel voting member at OASIS and an Intel representative to OASIS CPP/A Technical Committee. Before joining Intel, Tim was lead systems engineer for UK ASTOR (Airborne Standoff Radar) and lead systems engineer for the Strategic Technology Insertion Business Area at Motorola. He currently has one patent filed. Tim holds a B.S. in computer science (magna cum laude) from Arizona State University.

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Wireless

Developing 2.5G and 3G Cell Phones with Symbian OS and Intel® Platform

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Overview

Many of the capabilities of the mobile phone used by the heroine in the recent film *Lara Croft: Tomb Raider* are for the future, but the future is closer than most think. Close to 3 million developers (Symbian developers worldwide, Java* and WAP developers, and developers registered with cell phone manufacturers) are able to create software for devices that merge voice communications and wireless Internet access with computing functionality. They use solutions that combine Symbian OS (operating system) technology and a hardware platform such as the Intel® StrongARM* microprocessor or Intel® XScale™ microarchitecture. These solutions are available to all developers of Symbian OS phones.

Improved Performance, Shortened Development

The speed provided through Intel StrongARM SA-1100 microprocessors and Intel XScale microarchitecture improves the performance and shortens the development cycle for data-enabled cell phones. Development options span the spectrum from traditional PDAs (with handheld computer functionality and occasional communication) and data-enabled cell phones (with voice communication and enough data capability to support an address book and basic messaging).

Ericsson, Nokia, and Psion are already shipping these devices. Other manufacturers such as Kenwood, Motorola, Panasonic, Sony, and Siemens, are developing Symbian OS phones using these solutions. At the same time, key technology providers such as RealNetworks, PacketVideo, Oracle, and Beatnik are ensuring that cell phones have all the necessary functionality for a successful handheld communicator.

Symbian OS

Symbian OS is a common core of application program interfaces (APIs) and technology shared among all Symbian OS phones. It includes the kernel, middleware for communications, data management, and graphics and application engines. This technology is driving much of the current development of reference designs for communicators (like the Nokia 9290 Communicator) and smart phones (like the Ericsson 380 Smartphone).

The Nokia 9290 Communicator (for the US market) is a data-centric device with a keyboard for advanced text input, as well as fully-integrated voice functionality. The Ericsson R380 Smartphone, is more a voice-centric device, offering a browser for data retrieval and more limited text input.

Key Features of Symbian OS

- Supports a wide range of mobile phone form factors and user interfaces, including tablet- or keyboard-based text input
- Supports four program and content development options–C++, Java, WAP, and Web
- Closely integrates functions required by data-enabled cell phones–contacts information, messaging, browsing, and wireless telephony
- Communication protocols–TCP/IP, WAP, GSM, GPRS, Bluetooth*, IrDA, serial
- Security–full-strength encryption and certificate management, secure communications protocols, certificate-based application installation
- Rich suite of application engines, including contacts, schedule, messaging, browsing, voice, office, utility, and system control

- Worldwide locale support through Unicode characters, flexible text input framework, and additional font and text formatting support
- Support for data synchronization
- Support for open standards such as SyncML, Java, USB, SMS, and Bluetooth

Features of Symbian OS Architecture

- *Client-server architecture*–object-oriented design as shown in Figure 1
- *Multiple server functionality*–many small servers increase functionality
- *Plug-in modules*–enable developers to add their own features
- *Multiple telephony standards*–integrated telephony components that allow developers to move their products from one protocol to another

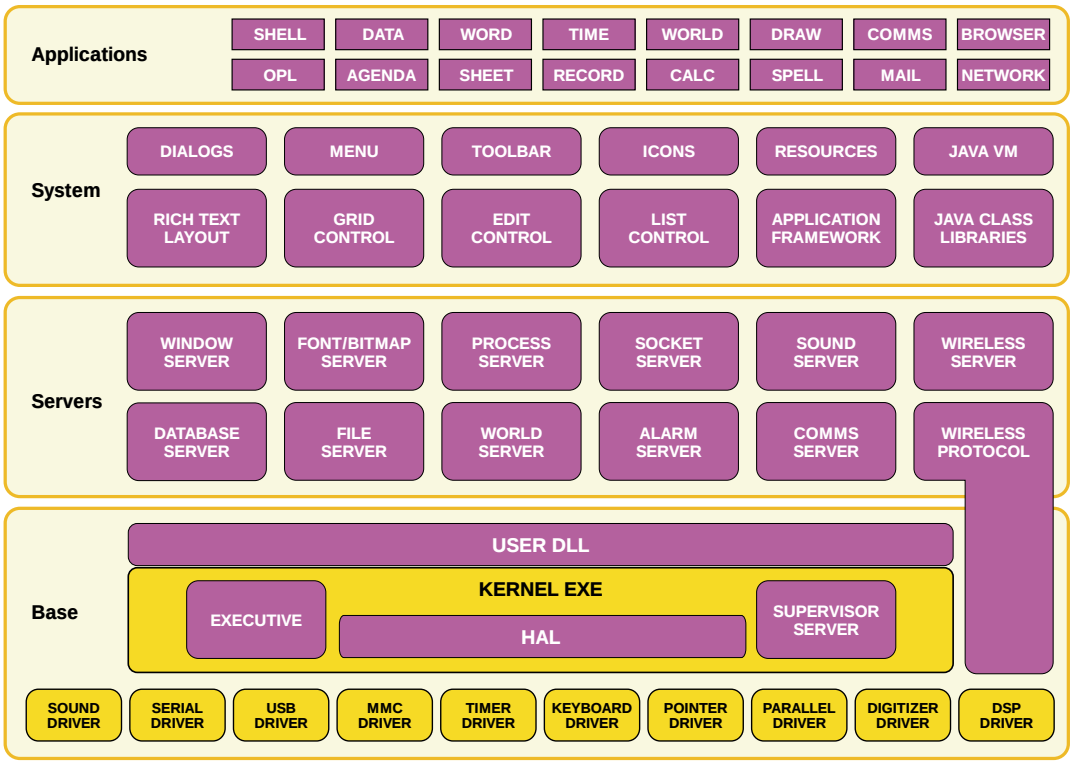

Figure 1. Symbian OS Client-Server Architecture

Symbian OS Designs

Both developing for a cell phone and developing the cell phone itself involve many considerations. Developers base their work on the kinds of applications and services that would be used on these phones. Other factors to take into account when developing a design include:

- Display–landscape or portrait orientation, color or grayscale, bit-depth (8-bit minimum, moving toward 16-bit), dot-pitch (0.19 mm to 0.22 mm)
- Navigation model–keyboard, keypad, touch screen, or combination
- Locale–languages supported via Unicode
- 2.5G or 3G network–GSM/GPRS, CDMA 1xRTT, WCMDA
- Application and browsing environments–Java, WAP, HTML

Symbian OS brings together the wireless value chain. It drives standards for the interoperation of data-enabled cell phones with mobile networks, content providers, and developers.

A Platform for Wireless Services: Symbian delivers an advanced, open, standard operating system to its cell phone manufacturers. It is flexible and scalable enough to be used in the variety of mobile phones needed to meet user requirements. Symbian OS supports complex requirements of network protocols worldwide and enables a broad, international developer community.

Providing Wireless Services: Network operators can customize Symbian OS phones for network-specific requirements, such as branding and customized or specialist services. Open standards ensure global network interoperability, allowing mobile phone users to communicate with anyone, in any way, at any time. The compelling advanced data services that operators can provide on Symbian OS phones will help minimize churn and maximize revenue.

Developing Wireless Services: Software developers are able to build applications and services for a global mass market of advanced, open, programmable, mobile phones. A set of standard application programming interfaces (APIs) across all Symbian OS phones and the advanced computing and communications capabilities enable development of ubiquitous services.

Summary

Packet-switched (2.5G and 3G) cell phone capabilities that may seem futuristic to many are actually being developed today. Cell phone manufacturers are creating advanced cell phones using solutions combining the Symbian OS with hardware platforms such as Intel StrongARM microprocessors or Intel XScale microarchitecture. These solutions are available to developers now.

More Info

For free SDKs in C++, Java, and Connectivity, visit the Symbian Developer Network Web site.

To learn more about Intel StrongARM specifications and hardware reference boards, visit the Intel Web site.

Attend the Symbian Developer Expo 2001 November 6–7 in Barcelona, Spain. To learn more, visit the Symbian Developer Expo 2001 Web site.

Author Bios

Gordon Bitko has been at Symbian for one year. He is responsible for developing relationships with key semiconductor partners. Prior to working at Symbian, he was a product manager for Motorola’s Semiconductor Products Sector. He has a B.S.E. from Princeton, an M.S. in control systems from the University of California, Berkeley, and an M.B.A. from Arizona State University.

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